Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Original) A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising: generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an indication of a site in at least one layer of the IC that is susceptible to a process fault; fabricating the at least one layer of the IC on the wafer; and applying a process monitoring tool to perform a measurement at the site in the at least one layer responsively to the PDP.

2. (Original) The method according to claim 1, wherein applying the process monitoring tool comprises measuring a dimension associated with one or more features of the IC at the site.

3. (Original) The method according to claim 1, wherein generating the PDP comprises making a determination that the site is critical to a performance rating of the IC, and selecting the site responsively to the determination.

4. (Original) The method according to claim 1, wherein generating the PDP comprises making a determination that the site is marginal with respect to a design rule of the IC, and selecting the site responsively to the determination.

5. (Original) The method according to claim 1, wherein generating the PDP comprises making a determination that the site is marginal with respect to a variation in a parameter of a process used in fabricating the IC, and selecting the site responsively to the determination.

6. (Original) The method according to claim 1, wherein generating the PDP comprises determining a mask error enhancement factor (MEEF) at the site, and selecting the site responsively to the MEEF.

7. (Original) The method according to claim 1, wherein generating the PDP comprises determining an optical proximity correction (OPC) to be applied at the site, and selecting the site responsively to the OPC.

8. (Original) The method according to claim 1, wherein generating the PDP comprises determining a density of structures in the IC at the site, and selecting the site responsively to the density.

9. (Original) The method according to claim 1, wherein the site comprises a location of a pair of matched circuit elements, and wherein applying the process monitoring tool comprises verifying that a critical characteristic of both the circuit elements in the pair is substantially identical.

10. (Original) The method according to claim 1, and comprising predicting a yield of the fabrication of the IC responsively to the PDP and to the measurement.

11. (Original) A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising: generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an identification of a region in at least one layer of the IC that is characterized by a periodic pattern; fabricating the at least one layer of the IC on the wafer; and applying a process monitoring tool to perform a measurement in the region of the at least one layer responsively to the periodic pattern.

12. (Original) The method according to claim 11, wherein generating the PDP comprises determining a pitch and a direction of the periodic pattern, and wherein applying the process monitoring tool comprises selecting a spatial filter responsively to the pitch and the direction, and performing optical inspection of the region using the spatial filter.

13. (Original) The method according to claim 11, wherein generating the PDP comprises determining a direction of the periodic pattern, and wherein applying the process monitoring tool comprises selecting a scan direction responsively to the direction of the periodic pattern, and inspecting the region while scanning over the region in the selected scan direction.

14. (Original) The method according to claim 11, wherein generating the PDP comprises determining an exact period of a repetitive feature in the periodic pattern, and wherein applying the process monitoring tool comprises capturing multiple images of the feature at locations on the wafer that are mutually spaced by the exact period, and comparing each of the images to another of the images or to a reference image.

15. (Original) The method according to claim 11, wherein applying the process monitoring tool comprises determining, responsively to the periodic pattern, a sensitivity setting to be applied by the process monitoring tool in detecting defects in the region, wherein different sensitivity settings are applied by the process monitoring tool in different regions of the at least one layer.

16. (Original) A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising: generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an identification of a plurality of regions in at least one layer of the IC and a respective criticality parameter for each of the regions, indicative of a maximum tolerable defect size in each of the regions; fabricating at least one layer of the IC on the wafer; and applying a process monitoring tool to perform a measurement in one or more of the regions in at least one layer responsively to the respective criticality parameter.

17. (Original) The method according to claim 16, wherein applying the process monitoring tool comprises setting a defect detection threshold in each of the one or more of the regions responsively to the respective criticality parameter.

18. (Original) The method according to claim 16, wherein applying the process monitoring tool comprises selecting the one or more of the regions to inspect responsively to the respective criticality parameter.

19. (Original) The method according to claim 16, wherein applying the process monitoring tool comprises detecting a defect in one of the regions, and classifying the defect responsively to the criticality parameter.

20. (Original) A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer, comprising: designing a layout of at least one layer of the IC using an electronic design automation (EDA) tool, at least one layer comprising a structure that is amenable to testing; generating a product design profile (PDP) using the EDA tool, the PDP comprising information regarding the structure; fabricating at least one layer of the IC on the wafer; and applying a process monitoring tool to perform a measurement on the structure in at least one layer, responsively the information in the PDP.

21. (Original) The method according to claim 20, wherein the structure comprises a dedicated test structure.

22. (Original) The method according to claim 21, wherein the dedicated test structure is located in a non-die area of the wafer.

23. (Original) The method according to claim 20, wherein the structure comprises multiple elongate parallel conductors, and wherein applying the process monitoring tool comprises testing an electrical continuity of the conductors.

24. (Original) The method according to claim 23, wherein testing the electrical continuity comprises applying an electrical charge at a first end of at least some of the conductors, and measuring the electrical charge at a second end of the conductors.

25. (Original) The method according to claim 20, wherein the structure comprises one or more contact openings in at least one layer, and wherein applying the process monitoring tool comprises directing an electron beam to irradiate the one or more contact openings, and measuring a specimen current responsively to the electron beam.

26 - 82. (Cancelled)